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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| In re Patent Application of | : | |
| FRED STACEY et al. | : | Examiner: Clemence Han |
| Serial No.: 09/819,941 | : | Group Art Unit: 2665 |
| Filed: March 27, 2001 | : | |

For: FLEXIBLE BUFFERING SCHEME
FOR MULTI-RATE SIMD PROCESSOR

# APPEAL BRIEF

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## I. REAL PARTY IN INTEREST

The real party in interest is Ciena Corporation, the assignee of record of the subject patent application.

## II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any prior or pending appeals, judicial proceedings or interferences which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

## III. STATUS OF CLAIMS

Claims 1 through 15 are currently pending and have been finally rejected. Appellants hereby appeal the rejections of Claims 1 through 15.

## IV. STATUS OF AMENDMENTS

No amendment was filed in the subject patent application subsequent to issuance of the Final Rejection on June 30, 2005.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

Appellants' invention, as recited in Claim 1, is directed to a single instruction, multiple data (SIMD) controller for processing a plurality of data streams in a digital subscriber line (DSL) system. (See Figure 3, reference numeral 36; Specification, p. 1, lines 2 to 5; and Specification, p. 3, lines 13 to 16) The single instruction, multiple data (SIMD) controller includes a plurality of circular buffer circuits that store data from the plurality of data streams having independent data rates (See Figure 2, reference numeral 20; Figure 3, reference numeral 20, Specification, Claim 1, lines 3 and 4) and a plurality of address generation circuits that access the data stored in the plurality of circular buffer circuits. (See Figure 2, reference numeral 20; Figure 3, reference numeral 20, Specification, Claim 1, lines 5 and 6) The single instruction, multiple data (SIMD) controller further includes a plurality of processor circuits that process the data accessed by the plurality of address generation circuits (See Figure 3, reference numeral 15; Specification, p. 3, lines 13 to 16) and a program control unit that controls the plurality of processor circuits with an instruction (See Figure 3, reference numeral 12; Specification, p. 3, lines 13 to 16).

Appellants' invention, as recited in Claim 8, is a method of processing a plurality of data streams in a digital subscriber line (DSL) system. (See Figure 3, reference numeral 36; Specification, p. 7, Claim 8, lines 1 and 2) The method includes the acts of: (i) calculating a plurality of input addresses for the plurality of data streams based on a plurality of input base addresses and a plurality of input offset addresses (See Figure 2, reference numeral 20; Specification, p. 7, Claim 8, lines 3 and 4); (ii) storing a plurality of data from the plurality of data streams according to the plurality of input addresses

(See Figure 2, reference numeral 20; Specification, p. 7, Claim 8, lines 5 and 6); (iii) calculating a plurality of processor addresses for the stored plurality of data based on a plurality of processor base addresses and a plurality of processor offset addresses (See Figure 2, reference numeral 20; Specification, p. 7, Claim 8, lines 7 and 8); (iv) processing, using a single instruction, the stored plurality of data according to the plurality of processor addresses (See Figure 2, reference numeral 20; Specification, p. 3, lines 17 to 19; and, Specification, p. 7, Claim 8, lines 9 and 10); (v) calculating a plurality of output addresses for the processed plurality of data based on a plurality of output base addresses and a plurality of output offset addresses (See Figure 2, reference numeral 20; Specification, p. 7, Claim 8, lines 11 and 12); (vi) outputting the processed plurality of data according to the plurality of output addresses (See Figure 2, reference numeral 20; Specification, p. 3, lines 13 to 20; and, Specification, p. 7, Claim 8, lines 13 and 14); and (vii) updating the plurality of input base addresses, the plurality of processor base addresses, and the plurality of output base addresses (See Figure 2, reference numeral 20; Specification, p. 7, Claim 8, lines 15 and 16).

Appellants' invention, as recited in Claim 9, is a single instruction, multi data (SIMD) architecture for controlling the processing of plurality of data streams (See Figure 3, reference numeral 36; Specification, p. 3, lines 13 to 16) and a memory that stores data from the plurality of data streams received from a plurality of channels (See Figure 3, reference numeral 20; Specification, p. 3, lines 13 to 16; and, Specification, p. 4, lines 19 to 24). The architecture also includes a processor operatively coupled with the memory (See Figure 3, reference numeral 15; Specification, p. 3, lines 13 to 16). The processor processes the data from the plurality of data streams (See Figure 3, reference

numeral 15; Specification, p. 3, lines 13 to 16). The architecture further includes a controller that controls the processor, wherein storing said data in the memory decouples a first operating rate of the processor and a second operating rate of the plurality of channels (See Figure 3, reference numeral 12; Specification, p. 3, lines 13 to 16; and, Specification, p. 4, lines 14 to 20).

Appellants' invention, as recited in Claim 11, is a method of controlling processing of multiple data streams in a single instruction, multi data (SIMD) architecture. (See Figure 3, reference numeral 36; Specification, p. 2, lines 16 to 21) The method includes the steps of: (i) storing data from the multiple data streams in a memory as the data is received (See Figure 3, reference numeral 36; Specification, p. 2, lines 16 to 21); (ii) at regular intervals, determining whether all of the data has been received (See Specification, p. 2, lines 16 to 21); (iii) providing a signal indicating that all of the data has been received (See Figure 3, reference numeral 36; Specification, p. 2, lines 16 to 21); (iv) using the signal to determine which of the data to process (See Figure 3, reference numeral 36; Specification, p. 2, lines 16 to 21); and, (v) processing the data in accordance with the signal (See Figure 3, reference numeral 36; Specification, p. 2, lines 16 to 21).

## VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are to be reviewed in the subject appeal:

(1) Whether Claims 8 through 12 are anticipated under 35 U.S.C. 102 (b) by U.S. Patent No. 5,410,727 (Jaffe et al.); and,

(2) Whether Claims 1 through 7 and 13 to 15 are obvious under 35 U.S.C. 103 from the combination of Jaffe et al. and U.S. Patent No. 5,448,706 (Fleming et al.).

## VII. ARGUMENT

Appellants respectfully submit that none of Claims 8 to 12 are anticipated by Jaffe et al. as Jaffe et al. fail to disclose expressly or inherently each and every element set forth in Claims 8 to 12. Accordingly, the rejection of Claims 8 to 12 cannot be sustained. Appellant further submits that none of Claims 1 through 7 and 13 to 15 are rendered obvious under 35 U.S.C. 103 by the combination of Jaffe et al. and Fleming et al. Because the necessary teaching, suggestion or motivation to combine these references is lacking, the rejection of Claims 1 through 7 and 13 through 15 is legally erroneous. Further, even if the unobvious combination of Jaffe et al. and Fleming et al. is made, Appellants' invention is still not rendered obvious. As such, the rejection of Claims 1 through 7 and 13 through 15 cannot be sustained.

### A. THE REJECTIONS OF CLAIMS 8 TO 12 ARE ERRONEOUS

#### 1. Claim 8 is not anticipated by Jaffe et al.

"Anticipation...requires that the *identical invention that is claimed* was previously known to others and thus is not new...." *Continental Can v. Monsanto,* 948 F.2d 1264, 1267 (Fed. Cir. 1991)(emphasis added). *A single reference must have each and every element of the claim.* See *Advanced Display Systems Inc. v. Kent State University*, 54 USPQ 2d 1673, 1679 (Fed. Cir. 2000)("Accordingly, invalidity by anticipation requires that the four corners of *a single, prior art document* describe every element of the claimed invention, expressly or inherently, such that *a person of ordinary skill in the art could practice the invention without undue experimentation.*")(emphasis added); See also, *PPG Industries, Inc. v. Guardian Industries Corp.*, 37 USPQ 2d 1618, 1624 (Fed. Cir. 1996)("To anticipate a claim, a reference must disclose every element of

the challenged claim and *enable one skilled in the art to make the anticipating subject matter.*")(emphasis added)

Claim 8 is not anticipated by Jaffe et al. as is readily evident from the Examiner's concessions. Specifically, the Examiner concedes that Jaffe et al. does not disclose a "digital subscriber line system." (See Official Action dated June 30, 2005, p. 9, ¶ 6)("Jaffe, however, does not teach a digital subscriber line system.") Contrary to the Examiner's assertion, the recitation "digital subscriber line system" appearing in the preamble of Claim 8 is a limitation as the preamble provides context essential to understand the meaning of terms in the body of the claim. Specifically, Claim 8 reads as follows:

> 8. A method of processing *a plurality of data streams* in a digital subscriber line (DSL) system, comprising the acts of:
>
> calculating a plurality of input addresses for *said plurality of data streams* based on a plurality of input base addresses and a plurality of input offset addresses;
>
> storing a plurality of data from *said plurality of data streams* according to said plurality of input addresses;
>
> calculating a plurality of processor addresses for the stored plurality of data based on a plurality of processor base addresses and a plurality of processor offset addresses;
>
> processing, using a single instruction, the stored plurality of data according to said plurality of processor addresses;
>
> calculating a plurality of output addresses for the processed plurality of data based on a plurality of output base addresses and a plurality of output offset addresses;
>
> outputting the processed plurality of data according to said plurality of output addresses; and
>
> updating said plurality of input base addresses, said plurality of processor base addresses, and said plurality of output base addresses. (emphasis added)

The preamble of Claim 8 expressly recites "a plurality of data streams." Further, *the first two clauses appearing in the body of Claim 8* include the recitation "*said* plurality of data streams." (emphasis added) *The preamble of Claim 8 provides the only antecedent basis for the two recitations "said plurality of data streams" appearing in the body of Claim 8.* Hence, the preamble is unquestionably a limitation of Claim 8 under the controlling precedent of the United States Court of Appeals for the Federal Circuit. See *Seachange International, Inc. v. C-Cor, Inc.*, 413 F.3d 1361 (Fed. Cir. (2005)("*The preamble provides the only antecedent basis and thus the context essential to understand the meaning of 'processor system'; therefore, the preamble, including the phrase 'distributed computer system,' limits the scope of the claimed invention.*")(emphasis added); See also, *C.R. Bard, Inc. v. M3Sys.*, 157 F.3d 1340, 1350 (Fed. Cir. 1998)("[A] preamble usually does not limit the scope of the claim *unless the preamble provides antecedents for ensuing claim terms and limits the claim accordingly.*") (emphasis added); and, *NTP, Inc., v. Research In Motion, Ltd.*, 392 F.3d 1336, 1358-1359 (Fed. Cir. 2004)

In *Seachange*, the Court had to determine whether the preamble of Claim 37 formed a limitation of the claim. Claim 37 is reproduced below:

> 37. A method for redundantly storing data in a distributed computer system having *at least three processor systems*, each processor system comprising at least one central processing unit and at least one mass storage sub-system, comprising the steps of:
>
> interconnecting each one of *said processor systems* through a network for data communications with each other one of *said processor systems*; and storing data input at any one of *said processor systems* according to a distributed, redundant storage process with data stored at each of *said processor systems* and a portion of a redundant representation of the data is stored at each of said processors. (emphasis added)

*In finding the preamble a limitation of the claim*, the Court explained, "[i]n this case, the preamble notes that the claimed method is for storing data in a 'distributed computer system' which has 'at least three processor systems'... The preamble further describes the components of a 'processor system' to be 'at least one central processing unit' and 'at least one mass storage subsystem'...The body outlines the claimed method, the steps of which repeatedly involve "said processor systems'... *The preamble provides the only antecedent basis and thus the context essential to understand the meaning of 'processor system'; therefore, the preamble, including the phrase 'distributed computer system,' limits the scope of the claimed invention.*" *Seachange*, 413 F.3d at 1375-1376. *Seachange* is indistinguishable from the present case as the preamble of Claim 8 of the subject patent application provides the only antecedent basis for the phrase *said plurality of data streams* appearing in the body of the claim. As such, the preamble is a limitation of the claim.

The Examiner's reliance on *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie,* 187 F. 2d 150, 152, 88 USPQ 478, 481 (CCPA 1951) is misplaced. In *Kropa,* the Court found the preamble to be a limitation. The Court explained in *Kropa that where the body of the claim is complete without the preamble, then the preamble is generally not a limitation. The body of Claim 8 is not complete as it expressly relies upon the preamble to provide antecedent basis for claim terms. In re Hirao* is readily distinguishable from the present case, as the preamble of the process claim at issue in that case was not needed to provide antecedent basis for any limitations appearing in the body of the claim.

The preamble of Claim 8 is a limitation of the claim as is readily evident from the controlling case law of the United Court of Appeals for the Federal Circuit. As such, Jaffe et al. admittedly does not anticipate Claim 8 since Jaffe et al. admittedly does not disclose expressly or inherently a DSL system. (See Official Action dated June 30, 2005, p. 9, ¶ 6)("Jaffe, however, does not teach a digital subscriber line system.")

Further, Jaffe et al. does not anticipate Claim 8 as it fails to disclose expressly or inherently the steps of calculating input addresses, output address and processing addresses using the corresponding base addresses and the corresponding offset addresses. In arguing that Jaffe et al does in fact disclose these steps, the examiner cites to Jaffe et al. at col. 7, lines 4 to 10; col. 10, lines 7 to 10; and col. 10, line 56 to col. 11, line 6. However, the Examiner's reliance on these passages is misplaced as these passages fail to disclose expressly or inherently the steps of calculating input addresses, output address and processing addresses *using the corresponding base addresses and the corresponding offset addresses*. Jaffe et al at col. 7, lines 4 to 10 merely refers to "segment starting address" and "segment length." Similarly, Jaffe et al. at col. 10, lines 7 to 10 merely refers to "SIMD starting address" and "SIMD length." Jaffe et al. at col. 10, line 56 to col. 11, line 6 merely states that the transfer of data from the SIMD to the buffers and from the buffers to the Host computer is the reverse action of the transfer of data from the host to the buffer and from the buffer to the SIMD. Accordingly, the Examiner has failed to establish a prima facie case of anticipation of Claim 8 by Jaffe et al. Appellants respectfully submit that the rejection of Claim 8 cannot be sustained.

**2. Claim 9 is not anticipated by Jaffe et al**

Applicants' invention, as recited in Claim 9, is directed to a single instruction, multi data (SIMD) architecture for controlling the processing of plurality of data streams having a memory that stores data from the plurality of data streams received from *a plurality of channels*. Claim 9 further recites a controller that controls the processor, wherein storing data in the memory *decouples a first operating rate of the processor and a second operating rate of the plurality of channels*. In rejecting Claim 9 on grounds of anticipation, the Examiner identifies memory 330 of Jaffe et al. However, the Examiner has failed to point out any passage in Jaffe et al. disclosing expressly or inherently that memory 330 stores data from the plurality of data streams *received from a plurality of channels*. For this reason alone, the Examiner has failed to establish a prima facie case that Jaffe et al. anticipates Claim 9.

With regard to the controller limitation of Claim 9, the Examiner points to Jaffe et al. at col. 7, lines 40 to 59. However, this passage of Jaffe et al. relied upon by the Examiner does not disclose expressly or inherently a controller that controls the processor, wherein storing data in the memory *decouples a first operating rate of the processor and a second operating rate of the plurality of channels*. As such, Jaffe et al cannot possibly anticipate Claim 9.

**3. Claim 10 is not anticipated by Jaffe et al**

Claim 10 recites that the plurality of data streams are carried in respective ones of the plurality of channels. The Examiner relies upon Jaffe et al. at col. 5, lines 59 to 66. However, this passage does not disclose expressly or inherently that the plurality of data streams are carried in respective ones of the plurality of channels.

**4. Claim 11 is not anticipated by Jaffe et al**

Appellants' invention, as recited in Claim 11, is directed to a method of controlling processing of multiple data streams in a single instruction, multi data (SIMD) architecture. The method includes the steps of: (i) storing data from the multiple data streams in a memory as the data is received; (ii) at regular intervals, determining whether all of the data has been received; (iii) providing a signal indicating that all of the data has been received; (iv) using the signal to determine which of the data to process; and (v) processing the data in accordance with the signal.

Appellants' respectfully submit that the Examiner has failed to establish a prima facie case that Jaffe et al. anticipates Claim 11. For step (i), the Examiner cites to Jaffe et al. at col. 9, lines 22 to 25. This passage of Jaffe et al. refers to the transfer of data from the host computer to the buffers (i.e., temporary storage). For steps (ii) and (iii), the Examiner cites to Jaffe et al at col. 8, lines 13 to 35. However, this passage merely explains the various components of the temporary storage means 310. Nowhere does this passage state expressly or inherently that it is determined at regular intervals whether all of the data has been received from the host computer. Further, this passage relied upon by the Examiner fails to disclose expressly or inherently the step of providing a signal indicating that all of the data has been received by the buffer from the host. For steps (iv) and (v) of Claim 11, the Examiner relies upon the following passage in Jaffe et al.:

> The input processor 320 is responsible for inputting the data from the buffers to the SIMD memory. The input/output processor 320 loads the address generation unit with "SIMD memory starting address" and "SIMD length" then invokes the address generation unit 350 to start the transfer. (See Jaffe et al. at col. 10, lines 7 to 11)

This section does not teach or suggest using a signal indicating that all of the data has been received in the memory to determine which of the data to process. Further, this section does not teach or suggest processing the data in accordance with the signal indicating that all of the data has been received in the memory. In fact, the above section of Jaffe et al. does not even mention a signal indicating that all of the data has been received. Accordingly, Jaffe et al. fails to disclose numerous limitations of Claim 11. As such, the Examiner's rejection of Claim 11 cannot be sustained.

**5. Claim 12 is not anticipated by Jaffe et al**

Claim 12 recites that the plurality of data streams are carried in respective ones of the plurality of channels. The Examiner relies upon Jaffe et al. at col. 5, lines 59 to 66. However, this passage does not disclose expressly or inherently that the plurality of data streams are carried in respective ones of the plurality of channels. Claim 12 is not anticipated by Jaffe et al. for this reason alone.

**B. THE REJECTIONS OF CLAIMS 1 TO 7 AND 13 TO 15 ARE ERRONEOUS**

The Examiner rejection of Claims 1 to 7 and 13 to 15 is under 35 USC § 103 based on the combination of Jaffe et al and Fleming et al. The law is well established on the issue of combining two or more references to render a claim unpatenable under 35 U.S.C. § 103. "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." In re Fine, 837 F.2d 1071, 5 USPQ 2d 1596, 1600 (Fed. Cir. 1988). See also Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 227 USPQ 543, 548 (Fed. Cir. 1985)("From its discussion of the prior art it appears to us that the court, guided by the defendants, treated each reference as teaching one or more of the specific components for use in the Feil system, although the

Feil system did not exist. Thus the court reconstructed the Feil system, using the blueprint of the Feil claims. As is well established, this is legal error.") *Accordingly, hindsight reconstruction is impermissible.* "When an obviousness determination is based on multiple references, there must be a showing of some 'teaching, suggestion, or reason' to combine the references...Although a reference need not expressly teach that the disclosure contained therein should be combined with another...the showing of combinability, in whatever form, must be '*clear and particular.*'" Winner International Royalty Corp. v. Wang, 202 F.3d 1340, 1348-1349 (Fed. Cir. 2000)(emphasis added). Hence, *there must be a clear and particular showing of the combinability of two or more references.*

When evaluated under these legal standards, the Examiner's rejections of Claims 1 to 7 and 13 to 15 cannot be sustained.

**1. Claim 1 is not rendered obvious by the combination of Jaffe et al and Fleming et al**

Even if Jaffe et al and Fleming et al. are combined, the combination does not render obvious Claim 1 reproduced below:

> A single instruction, multiple data (SIMD) controller for processing *a plurality of data streams in a digital subscriber line (DSL) system*, comprising:
>
> a plurality of circular buffer circuits that store data from *said plurality of data streams* having independent data rates;
>
> a plurality of address generation circuits that access said data stored in said plurality of circular buffer circuits;
> a plurality of processor circuits that process said data accessed by said plurality of address generation circuits; and
>
> a program control unit that controls said plurality of

processor circuits with an instruction.

Claim 1, like Claim 8 previously discussed, includes the phrase "a plurality of data streams in a digital subscriber line (DSL) system" in the preamble. Claim 1, also like Claim 8, includes *in the body of the claim* the recitation "said plurality of data streams." The only antecedent basis for the limitation "said plurality of data streams" is found in the preamble. As such, the preamble is a limitation of Claim 1. See *Seachange International, Inc.*, 413 F.3d 1361; *C.R. Bard, Inc..*, 157 F.3d at 1350; and, *NTP, Inc.*, 392 F.3d at 1358-1359. Both Jaffe et al and Fleming et al fail to teach or suggest the digital subscriber line (DSL) system limitation of Claim 1. For this reason alone, the Examiner's rejection of Claim 1 cannot be sustained.

Further, because the necessary teaching, suggestion or motivation to combine Jaffe et al and Fleming et al. is lacking, the Examiner's rejection of Claim 1 cannot be sustained. Jaffe et al. is directed to an input/output system for a massively parallel, single instruction, multiple data (SIMD) computer providing for the simultaneous transfer of data between a host computer input/output system and all SIMD memory devices. Admittedly, Jaffe et al. does not disclose a circular buffer. (See Official Action dated June 30, 2005, p. 4, ¶ 3)("Jaffe, however, does not teach the circular buffer that stores data from said plurality of data streams having independent data rates.") *Perhaps more importantly, Jaffe et al. does not disclose processing that would utilize a circular buffer.* In other words, there is simply no reason to modify Jaffe et al. to include a circular buffer as Jaffe et al has no use for a circular buffer. Fleming et al. does not teach or suggest modifying a SIMD architecture of Jaffe et al to perform processing that would utilize a circular buffer. Rather, Fleming et al merely teaches a method of generating a sequence

of address signals for use in a digital signal processing system *where the system performs circular buffer style processing.* (See Fleming et al. col. 1, lines 8 to 14) It is undisputed that the system in Jaffe et al. does not perform circular buffer style processing. As such, there is no teaching, suggestion or motivation to combine Fleming et al. designed for systems with circular buffer style processing with a SIMD architecture of Jaffe et al. that has absolutely no use for circular buffer style processing. Accordingly, Appellants respectfully submit that Claim 1 is patentable.

**2. Claim 2 is not rendered obvious by the combination of Jaffe et al and Fleming et al**

Claim 2 depends from Claim 1 and further recites that the plurality of circular buffer circuits include a first section that stores the one or more symbols before being processed, a second section that stores the one or more symbols being processed and a third section that stores one or more symbols. In an attempt to meet these limitations, the Examiner points solely to Jaffe et al. (See Official Action dated June 30, 2005, p. 5) The Examiner's reliance on Jaffe et al is clearly misplaced as this reference does not even teach a circular buffer let alone the specific structure for the plurality of circular buffer circuits set forth in Claim 2. Hence, the Examiner's rejection of Claim 2 cannot possibly be sustained.

**3. Claim 3 is not rendered obvious by the combination of Jaffe et al and Fleming et al**

Claim 3 depends from Claim 1 and further recites that one of the plurality of address generation circuits include, *inter alia*, a symbol manager circuit that generates a input *base* address, a processor *base* address and an output *base* address wherein the one of the plurality of address generation circuits receives an input *offset* address, a processor

*offset* address and an output *offset* address. In arguing that these limitations are found in the prior art, the Examiner cites to Jaffe et al at col. 6, line 61 to col. 7, line 23. However, this passage relied upon by the Examiner merely refers to a "segment starting address" and a "segment length." Nowhere does Jaffe et al or Fleming et al teach the limitations of Claim 3 including but not limited to the base addresses and offset addresses. Accordingly, the Examiner's rejection of Claim 3 cannot be sustained.

**4. Claim 4 is not rendered obvious by the combination of Jaffe et al and Fleming et al**

Claim 4 depends from Claim 1 and recites that the plurality of processor circuits further receive a plurality of enable signals and selectively process the data based on the plurality of enable signals. The Examiner's proposed combination does not teach or suggest this feature of Appellants' invention. The Examiner points to Jaffe et al at col. 8, lines 13 to 35. The enable signal referred to in this section of Jaffe et al merely enables the buffer for loading or storing. Nowhere does Jaffe et al teach or suggest that the plurality of processor circuits receive a plurality of enable signals and selectively process the data based on the plurality of enable signals. Accordingly, the Examiner's rejection of Claim 4 cannot be sustained.

**5. Claim 5 is not rendered obvious by the combination of Jaffe et al and Fleming et al**

Claim 5 depends from Claim 1 and recites that the plurality of address generation circuits further selectively generate a plurality of enable signals, depending upon whether a full symbol is ready for processing in each of the plurality of address generation circuits. The Examiner's proposed combination does not teach or suggest this feature of Appellants' invention. The Examiner points to Jaffe et al. at col. 8, lines 13 to 35. The

enable signal referred to in this section of Jaffe et al merely enables the buffer for loading or storing. Nowhere does Jaffe et al teach or suggest that the plurality of address generation circuits further selectively generate a plurality of enable signals, depending upon whether a full symbol is ready for processing in each of the plurality of address generation circuits. Accordingly, the Examiner's rejection of Claim 5 cannot be sustained.

**6. Claim 6 is not rendered obvious by the combination of Jaffe et al and Fleming et al**

Claim 6 depends from Claim 5 and recites that the plurality of processor circuits further receive a plurality of enable signals and selectively process the data based on the plurality of enable signals. The Examiner's proposed combination does not teach or suggest this feature of Appellants' invention. The Examiner points to Jaffe et al. at col. 8, lines 13 to 35. The enable signal referred to in this section of Jaffe et al merely enables the buffer for loading or storing. Nowhere does Jaffe et al teach or suggest that the plurality of processor circuits receive a plurality of enable signals and selectively process the data based on the plurality of enable signals. Accordingly, the Examiner's rejection of Claim 6 cannot be sustained.

**7. Claim 7 is not rendered obvious by the combination of Jaffe et al and Fleming et al**

Claim 7 depends from Claim 1 and recites that the plurality of address generation circuits further selectively generate a plurality of enable signals, depending upon a difference between an input base address and a processor base address in each of the plurality of address generation circuits. The Examiner's proposed combination does not teach or suggest this feature of Appellants' invention. The Examiner points to Jaffe et al.

at col. 8, lines 13 to 35. The enable signal referred to in this section of Jaffe et al merely enables the buffer for loading or storing. Nowhere does Jaffe et al teach or suggest that the plurality of address generation circuits further selectively generate a plurality of enable signals, depending upon a difference between an input base address and a processor base address in each of the plurality of address generation circuits. Accordingly, the Examiner's rejection of Claim 7 cannot be sustained.

**8. Claim 13 is not rendered obvious by the combination of Jaffe et al and Fleming et al**

Claim 13 depends from Claim 11 and recites that the multiple data streams have independent data rates. Appellants respectfully submit that there is no teaching, suggestion or motivation to modify the SIMD architecture of Jaffe et al such that multiple data streams have independent data rates. Fleming et al has nothing whatsoever to do with the SIMD architecture of Jaffe et al. Specifically, Fleming et al teaches a method of generating a sequence of address signals for use in a digital signal processing system *where the system performs circular buffer style processing.* (See Fleming et al, col. 1, lines 8 to 14) The SIMD system in Jaffe et al does not perform any circular buffer style processing. As such, there is simply no reason to combine these divergent teachings. Appellants' further submit that the only way this combination can be made is through the use of impermissible hindsight reconstruction. Thus, the Examiner's rejection of Claim 13 cannot be sustained.

**9. Claim 14 is not rendered obvious by the combination of Jaffe et al and Fleming et al**

Claim 14 depends from Claim 9 and recites that the plurality of data streams have independent data rates. Appellants respectfully submit that there is no teaching, suggestion or motivation to modify the SIMD architecture of Jaffe et al such that a plurality of data streams have independent data rates. Fleming et al has nothing whatsoever to do with the SIMD architecture of Jaffe et al. Specifically, Fleming et al teaches a method of generating a sequence of address signals for use in a digital signal processing system *where the system performs circular buffer style processing.* (See Fleming et al, col. 1, lines 8 to 14) The SIMD system in Jaffe et al does not perform any circular buffer style processing. Hence, there is no reason to combine these divergent teachings. Appellants' further submit that the only way this combination can be made is through the use of impermissible hindsight reconstruction. Thus, the Examiner's rejection of Claim 14 cannot be sustained.

**10. Claim 15 is not rendered obvious by the combination of Jaffe et al and Fleming et al**

Claim 15 depends from Claim 8 and recites that the plurality of data streams have independent data rates. Appellants respectfully submit that there is no teaching, suggestion or motivation to modify the SIMD architecture of Jaffe et al such that a plurality of data streams have independent data rates. Fleming et al has nothing whatsoever to do with the SIMD architecture of Jaffe et al. Specifically, Fleming et al teaches a method of generating a sequence of address signals for use in a digital signal processing system *where the system performs circular buffer style processing.* (See Fleming et al, col. 1, lines 8 to 14) The SIMD system in Jaffe et al does not perform any

circular buffer style processing. As such, there is simply no reason to combine these divergent teachings. Appellants' further submit that the only way this combination can be made is through the use of impermissible hindsight reconstruction. Thus, the Examiner's rejection of Claim 15 cannot be sustained.

**C. CONCLUSION**

When evaluated under the controlling legal standards, the Examiner's rejections of Claims 1 through 15 cannot be sustained. Hence, Appellants respectfully request that all grounds of rejection be reversed.

A check in the amount of $500.00 is attached hereto to satisfy the government fee for filing the subject appeal brief. It is believed that no additional fees are due. However, should that determination be incorrect, the Commissioner is hereby authorized to charge any deficiencies to Deposit Account No. 50-0562 and notify the undersigned in due course.

Respectfully submitted,

Date: 12/13/05

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## VIII. CLAIMS APPENDIX

1. A single instruction, multiple data (SIMD) controller for processing a plurality of data streams in a digital subscriber line (DSL) system, comprising:

a plurality of circular buffer circuits that store data from said plurality of data streams having independent data rates;

a plurality of address generation circuits that access said data stored in said plurality of circular buffer circuits;

a plurality of processor circuits that process said data accessed by said plurality of address generation circuits; and

a program control unit that controls said plurality of processor circuits with an instruction.

2. The controller of claim 1, wherein one of said plurality of circular buffer circuits comprises:

a first section that stores one or more symbols before being processed;

a second section that stores said one or more symbols being processed; and

a third section that stores said one or more symbols after being processed.

3. The controller of claim 1, wherein one of said plurality of address generation circuits comprises:

a symbol manager circuit that generates an input base address, a processor base address, and an output base address,

wherein said one of said plurality of address generation circuits further receives an input offset address, a processor offset address, and an output offset address, and generates an input address, a processor address, and an output address in accordance with said input base address, said processor base address, and said output base address.

4. The controller of claim 1, wherein said plurality of processor circuits further receive a plurality of enable signals and selectively process said data based on said plurality of enable signals.

5. The controller of claim 1, wherein said plurality of address generation circuits further selectively generate a plurality of enable signals, depending upon whether a full symbol is ready for processing in each of said plurality of address generation circuits.

6. The controller of claim 5, wherein said plurality of processor circuits further receive said plurality of enable signals and selectively process said data based on said plurality of enable signals.

7. The controller of claim 1, wherein said plurality of address generation circuits further selectively generate a plurality of enable signals, depending upon a difference between an input base address and a processor base address in each of said plurality of address generation circuits.

8. A method of processing a plurality of data streams in a digital subscriber line (DSL) system, comprising the acts of:

calculating a plurality of input addresses for said plurality of data streams based on a plurality of input base addresses and a plurality of input offset addresses;

storing a plurality of data from said plurality of data streams according to said plurality of input addresses;

calculating a plurality of processor addresses for the stored plurality of data based on a plurality of processor base addresses and a plurality of processor offset addresses;

processing, using a single instruction, the stored plurality of data according to said plurality of processor addresses;

calculating a plurality of output addresses for the processed plurality of data based on a plurality of output base addresses and a plurality of output offset addresses;

outputting the processed plurality of data according to said plurality of output addresses; and

updating said plurality of input base addresses, said plurality of processor base addresses, and said plurality of output base addresses.

9. A single instruction, multi data (SIMD) architecture for controlling the processing of plurality of data streams, comprising:

a memory that stores data from said plurality of data streams received from a plurality of channels;

a processor, operatively coupled with said memory, that processes said data from said plurality of data streams; and

a controller that controls said processor, wherein storing said data in said memory decouples a first operating rate of said processor and a second operating rate of said plurality of channels.

10. A SIMD architecture as defined in claim 9, wherein said plurality of data streams are carried in respective ones of said plurality of channels.

11. A method of controlling processing of multiple data streams in a single instruction, multi data (SIMD) architecture, comprising the steps of:

storing data from said multiple data streams in a memory as said data is received;

at regular intervals, determining whether all of said data has been received;

providing a signal indicating that all of said data has been received;

using said signal to determine which of said data to process; and

processing said data in accordance with said signal.

12. A method as defined in claim 11, wherein said multiple data streams are carried in respective ones of a plurality of channels.

13. The method of claim 11, wherein said multiple data streams have independent data rates.

14. The SIMD architecture of claim 9, wherein said plurality of data streams have independent data rates.

15. The method of claim 8, wherein said plurality of data streams have independent data rates.

## IX. EVIDENCE APPENDIX

None.

## X. RELATED PROCEEDINGS APPENDIX

None.